

# A Configurable Decoder for Pin-Limited Applications

Flexible, efficient translation of pin-limited input signals to multiple output signals in FPGAs, integrated circuits or DSP chipsets

**Patent Status:** In Prosecution

**Technology Status:** Simulation

**Terms:** Exclusive or Non-Excl

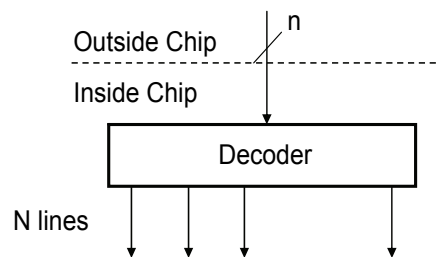
**Availability:** Immediate

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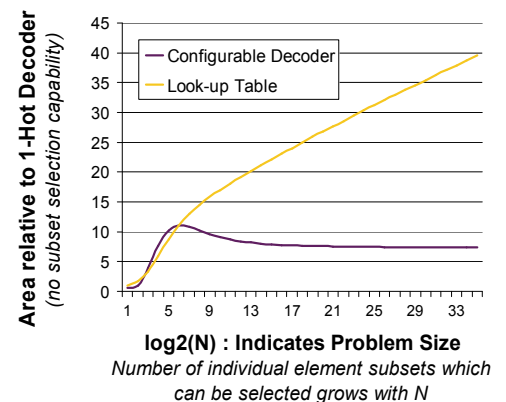
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Process of configurable signal decoding, by configuring the array one column at a time. Decoder is small but vital part of system.

Invention provides high area efficiency



**Processor speeds have increased much faster than rates at which data can enter and leave a chip.**

Pin limitations are a major performance and size bottleneck in IC chips, particularly FPGAs. To solve this, chips use input decoding, where a few input bits drive internal selection of a subset from a large number of elements. Prevalent fixed 1-hot decoders are inexpensive and can quickly choose one element. However, this one-by-one selection results in a slow solution over multiple applications. A key requirement for FPGAs is fast yet flexible selection of elements in a manner tailored to the application at hand. Prevalent solutions are based on look-up table (LUT) decoding, which is flexible but expensive.

Our configurable decoder solution offers both the economy and speed of fixed decoders and the flexibility of LUT-based decoders. It scales effectively for large problem sizes. An adaptation of this invention can lower implementation costs of conventional fixed decoders.

Simulations are available for demonstration. This mature technology can be immediate commercialized.

## Advantages

- **Fast signal translation**  
Speed comparable to conventional fixed decoders
- **Low adoption barrier**  
Lowers cost for current fixed decoder implementations
- **Flexible**  
Decoder function configurable to match application needs
- **Low gate cost**  
Comparable to 1-hot decoder and much lower than LUT
- **No end-user impact**  
Unchanged user-side interface

